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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,991	09/09/2004	Shigeho Inatsune	257416US2PCT	1935

22850 7590 06/19/2006

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EXAMINER	
SOTOMAYOR, JOHN B	
ART UNIT	**PAPER NUMBER**
3662	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/506,991	INATSUNE, SHIGEHO	
	Examiner	Art Unit	
	John B. Sotomayor	3662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 3 is/are allowed.

6)☒ Claim(s) 1,2 and 4-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 September 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09SEP04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings filed September 9, 2004 appear to be formal and are acceptable.

3. Figures 11-15, 16a, 16b, 17a, 17b, 18a and 18b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

4. The information disclosure statement filed September 9, 2004 has been entered and considered. An initialed copy of the PTO-1449 by the Examiner is attached.

5. The information disclosure statement filed October 20, 2005 has been entered and considered. An initialed copy of the PTO-1449 by the Examiner is attached.

Preliminary Amendment

6. The preliminary amendment filed September 9, 2004 has been entered and considered. An initialed copy of the PTO-1449 by the Examiner is attached.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2 and 4-7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Caldwell et al ('661) or Budzelaar ('567) or Shimada et al ('017) or Akashi et al ('307).

Clearly the prior art, as exemplified by Caldwell et al ('661), is considered to meet the claim language as recited by disclosing: a waveform generating system including, inter alia, timing the output of a D/A converter so that the output voltage is almost constant.

Caldwell et al ('661) disclose, referring to FIG. 4 reproduced below,

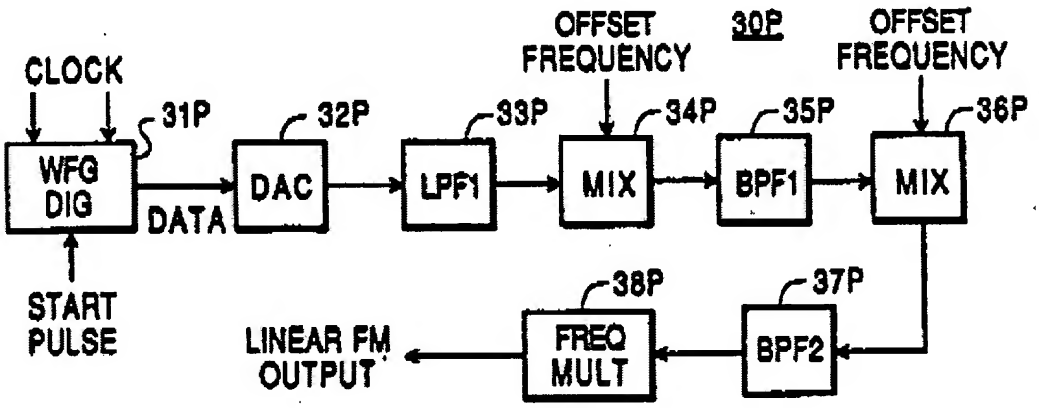


FIG. 4
PRIOR ART

a clock timing section with start pulse, D/A converter 32P, and low pass filter 33P.

Clearly the prior art, as exemplified by Budzelaar ('567), is considered to meet the claim language as recited by disclosing: a waveform generating system including, inter alia, timing the output of a D/A converter so that the output voltage is almost constant.

Budzelaar ('567) disclose a multiple-output digital to analog converter having a waveform generator WG, a timing generator TG converts digital input data Dd into a plurality of control signals Csi determining time periods T1i during which corresponding switching elements Si are closed. Output voltages Voi across the associated loads Li vary according to the first waveform Wf1 until an associated switching element Si opens in conformity with the digital input data Dd. The waveform generator WG comprises a

second output O2 to supply a second waveform Wf2 of substantially the same shape as the first waveform Wf1. The multiple-output digital to analog converter further comprises a plurality of dummy loads Ldi, each one of the dummy loads Ldi is associated with one of the loads Li. The dummy loads Ldi are coupled to the second output O2 during the time periods Ti2 during which the corresponding switching elements Si are closed. In this way, the supply voltages Vdi across the dummy loads Ldi are substantially equal to the output voltages Voi across the associated loads Li. The dummy loads Ldi are coupled to the first output O1 when the corresponding switching elements Si are open. In this way, the load on the first output O1 is substantially constant.

Clearly the prior art, as exemplified by Shimada et al ('017), is considered to meet the claim language as recited by disclosing: a waveform generating system including, inter alia, timing the output of a D/A converter so that the output voltage is almost constant.

Shimada et al ('017) disclose switching is made in synchronization with a clock at a digital-to-analog converter to a constant current source or constant voltage source corresponding to each weight of digital value. If the switching timing is shifted, a glitch pulse occurs. Such glitch pulse is to be removed by interpolation by an interpolation filter through sampling at points shifted in output phase of the digital-to-analog converter. Since the present embodiment is constructed so as to match the sampling timing at the correction circuit and the sampling timing at the LCD drive circuit in the

manner as described above, deglitch processing and interpolation filter become unnecessary at the digital-to-analog conversion section.

Clearly the prior art, as exemplified by Akashi et al ('307), is considered to meet the claim language as recited by disclosing: a waveform generating system including, inter alia, timing the output of a D/A converter so that the output voltage is almost constant.

Akashi et al ('307) disclose U.S. Pat. No. 2,907,021 discloses a D/A converter which receives an input digital signal and generates a pulse with the pulse width varied in accordance with the input signal, which pulse switches a reference voltage to generate a pulse signal with a constant voltage amplitude which is in turn filtered by means of a low-pass filter thereby to obtain a direct current signal (which will be shortly referred to as a "DC signal"). In a PWM pulse generator used in the D/A converter disclosed, the value of a counter made operative for a constant period is compared with an input digital signal and the PMW signal corresponding to the input digital signal is fed out. More specifically, a flip-flop is reset at a timing corresponding to a repetition period, e.g., when the value of the counter becomes 0. The flip-flop is set when the value of the counter and the input digital signal are compared and found to be coincident. By these operations, a signal having a pulse width which is proportional to the digital input signal value is generated. The generated signal is smoothed to obtain a DC voltage which has a value corresponding to the product of the reference voltage the ratio of the pulse width to the repetition period. As is apparent from the conversion principle, the accuracy of the output DC voltage is dependent upon the accuracy of the ratio of the pulse to the

repetition period. Therefore, it is made possible to obtain a highly accurate D/A converter by increasing the bit number of the counter. Hence an increase in the bit number is accompanied with a rise of the clock frequency for digital synchronized circuits such as the counter or a drop of the generated pulse frequency (i.e., the elongation of the duration of the repetition period). A rise of a clock frequency and the drop of the generated pulse frequency are both undesirable, because the switching speed of field effect transistors used in large-scale integration circuits is relatively low and therefore the clock frequency cannot be raised without introducing noise, and the drop of the repetition frequency of the generated pulse necessitates the increase in the time constant of a low-pass filter for smoothing the generated pulse so that the size of the low-pass filter will be enlarged.

Allowable Subject Matter

9. Claim 3 is allowed.

Conclusion

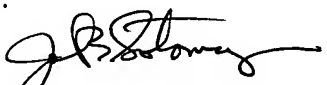
10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art is cited to show various radar systems.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Sotomayor whose telephone number is 571-

272-6978. The examiner can normally be reached on Monday to Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom H. Tarcza, can be reached on 571-272-6979. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Sotomayor
Primary Examiner
Art Unit 3662